

Sub B17

1. A signal routing apparatus, comprising:
a register bank to store a set of data signals;
5 a delay locked loop to generate a set of phase displaced clock signals;
a phase controlled read circuit to sequentially route said set of data signals
from said register bank in response to said phase displaced clock signals; and
a Low Voltage Differential Signaling buffer connected to said phase controlled
read circuit to transmit said data signals in a Low Voltage Differential Signaling mode.
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2. The signal routing apparatus of claim 1 wherein said phase controlled read
circuit includes a set of transistor columns, each transistor column of said set of
transistor columns being responsive to two phase displaced clock signals of said set of
phase displaced clock signals.
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3. The signal routing apparatus of claim 2 wherein each transistor column of said
set of transistor columns includes a subset of pull-up transistors connected to an output
node, said subset of pull-up transistors processing a first phase displaced clock signal,
a second phase displaced clock signal immediately adjacent to said first phase
20 displaced clock signal, and a register bank signal.
4. The signal routing apparatus of claim 3 wherein each transistor column of said
set of transistor columns includes a subset of pull-down transistors connected to said
output node, said subset of pull-down transistors processing a first phase displaced
25 clock signal, a second phase displaced clock signal immediately adjacent to said first
phase displaced clock signal, and a register bank signal.
5. The signal routing apparatus of claim 1 in combination with a programmable
logic device.
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6. The signal routing apparatus of claim 5 wherein said programmable logic
device is connected to a system bus.

7. The signal routing apparatus of claim 6 wherein a memory is connected to said system bus.

8. The signal routing apparatus of claim 6 wherein a processor is connected to said system bus.

9. The signal routing apparatus of claim 6 wherein input/output circuitry is connected to said system bus.

10. The signal routing apparatus of claim 6 wherein a peripheral device is connected to said system bus.

11. A method of routing signals, comprising:
storing a set of data signals;
generating a set of phase displaced clock signals;
sequentially routing said set of data signals in response to said phase displaced clock signals to form sequentially routed signals; and
transmitting Low Voltage Differential Signaling mode signals corresponding to said sequentially routed signals.

12. The method of claim 11 wherein said storing step includes the step of storing said set of data signals in a register bank.

13. The method of claim 11 wherein said generating step includes the step of generating said set of phase displaced clock signals with a delay locked loop.

14. The method of claim 11 wherein said routing step includes the step of sequentially activating a set of transistor columns in response to said phase displaced clock signals.

15. A signal routing apparatus, comprising:

